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Research Article

Single-Stage Coupled-Inductor Sepic-Type HB-LED Driver with Soft Switching for Universal Line Input

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This paper proposes a single-stage Sepic-type high brightness LED driver for universal line input to perform power factor correcting and LED dimming. In the driver, a coupled inductor is introduced to replace with two separate inductors to lower volume and cost. A soft-switching cell is embedded into the driver to obtain zero-voltage switching (ZVS) feature so as to furthermore improve driver efficiency. Mathematical derivation and detailed discussion is presented. A prototype is designed, analyzed and implemented, which demonstrates the feasibility of the driver and verifies the theoretical analysis.

1. Introduction

Power electronic devices with front-end rectifier are widely used in industry, commerce, and transportation, which generate current harmonics, produce power pollution, and result in low power factor. Therefore, there are international harmonic standards (such as IEC-1000 and IEC-555) to confine power pollution. In order to meet the requirements of the standards, the input current waveform of a device has to be shaped by a power factor corrector (PFC) to eliminate current harmonics and improve power factor.

The PFCs can be briefly classified into two types. One is passive and the other is active. Passive-type PFC is mainly constructed by inductors and capacitors. Low efficiency, heavy weight, and large volume are its major disadvantages. Besides, in general power factor merely is improved to around 0.8. For active type, active switch, diode and energy-stored component are used to achieve near unity power factor, of which topologies have Buck, Boost, Buck-Boost, ′Cuk, Zeta, Sepic, and Flyback. Conventional Buck-type PFC can obtain

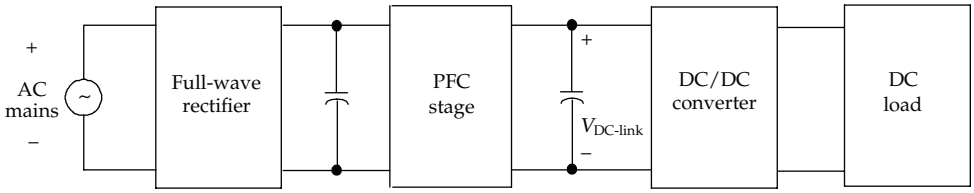

Figure 1: A PFC stage cascaded with a full-wave rectifier in the input and a step-down dc/dc converter in the output.

an output voltage smaller than ac input voltage. However, only a power factor of 0.95 is met [1]. The Boost structure attains better power factor correction feature but its output voltage is higher than ac-side voltage, and power components withstand high voltage stresses [2, 3]. The Buck-Boost PFC can obtain an output voltage magnitude either larger or smaller than the input. Nevertheless, there is a polarity reversal on the output, and an isolation driver for active switch is required [4, 5]. The 'Cuk, Zeta, Sepic, and Flyback topologies can resolve the problems caused from the Buck-Boost. Among them the Sepic type possesses better performance in total harmonics distortion (THD), efficiency, and power factor correction [6–13]. However, the Sepic PFC needs two separate inductors like 'Cuk and Zeta.

In this paper a dsPIC-based coupled-inductor Sepic-type converter for high-brightness light-emitting-diode (HB LED) lighting applications is presented, which can not only step down input voltage directly but also perform power factor correcting, drive LED panel, and complete dimming function. A soft-switching cell is proposed to reduce switching losses, improving efficiency. In addition, a bypass circuit in parallel with each LED is also proposed, which is cost-effective and suitable for IC process. A dual-loop control approach, which contains inner control loop and outer control loop to shape input current and to regulate output voltage, is also presented. In LED panel, the current of each LED string is sensed and controlled to accomplish current sharing and dimming feature. A 100 W prototype is designed, analyzed, and implemented. Simulations and practical results have demonstrated the feasibility of the single-stage Sepic-type LED driver and verified the aforementioned functions.

2. Power Stage Configuration

For high mains voltage or in low output voltage application, in general a Boost-type PFC is cascaded with a full-wave rectifier in the input and a step-down dc/dc converter in the output, as shown in Figure 1. The PFC stage shapes a high-crest-factor current caused by the full-wave rectifier into a purely sinusoidal waveform in phase with line voltage. However, the input voltage also is boosted. Therefore, it is required that a dc/dc converter is adopted to drop voltage for dc load. Power is processed by two stages, a PFC and a dc/dc converter, lowering overall efficiency and increasing cost. To release the mentioned drawbacks, a single-stage step-down PFC is adopted to simplify the structure of power-conversion stage, as shown in Figure 2, in which the PFC stage performs power factor correcting as well as steps down its input voltage to a desired level. In this paper, a dsPIC-based Sepic-type configuration is presented to serve as the single-stage step-down PFC for HB-LED driving, as shown in Figure 3. Figure 4 shows the corresponding main-stage schematic, in which the diodes D_5 and D_6 are introduced to prevent opposite current from flowing through inductors

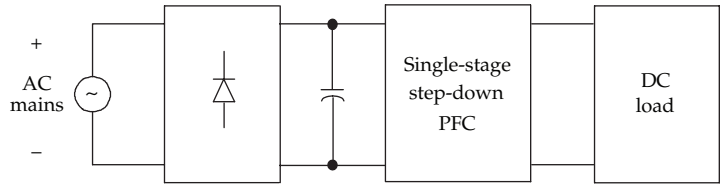

Figure 2: A block diagram representing single-stage step-down PFC.

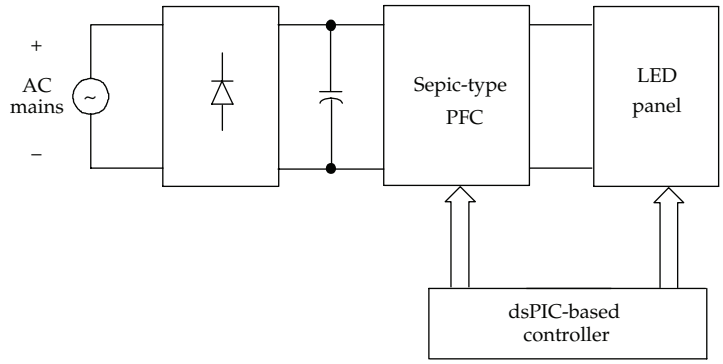

Figure 3: A block diagram representing that Sepic-type converter serves as PFC for LED lighting application.

L_1 and L_2, respectively. In Figure 4, the two separate inductors L_1 and L_2 can be coupled magnetically. In addition, a proposed soft-switching cell, including an active switch Q_2, an inductor L_r, and a capacitor C_r, to achieve zero-voltage switching (ZVS) feature, is embedded into the power stage to reduce switching loss. Figure 5 is the derived single-stage coupled-inductor soft-switching Sepic-type HB-LED driver.

3. Operation Principle of Power Stage

In Figure 5, while the soft-switching Sepic-type HB-LED driver operates in boundary conduction mode and with peak current control, a high power factor can readily be achieved. As a result, the envelope of the input current will follow the shape of line voltage to be sinusoidal, leading to unity power factor. As the resonant frequency of the soft-switching cell is much higher than switching frequency of main power circuit, over a switching cycle the operation of the driver can be divided into eight modes. Figure 6 is the corresponding circuits, and the related conceptual key waveforms are shown in Figure 7. The eight operation modes during a switching period are discussed as follows.

(1) Mode 1 ($t_0 \leq t < t_1$, Figure 6(a))

During this time interval, switch Q_1 is on and Q_2 off. The inductor currents of i_{L_1} and i_{L_r} are linearly built, and the capacitor C_2 dumps energy to inductor L_2 by the way of L_r, Q_1, and D_6. At the same time, the capacitor C_3 supplies power for load. The time constant determined by capacitance of C_3 and load resistance is much larger than switching period so that output

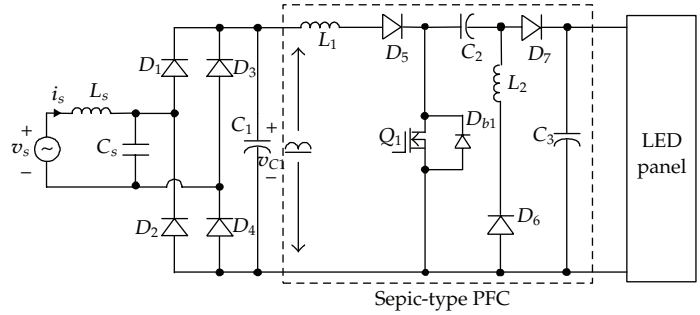

Figure 4: The main-stage schematic of a Sepic-type PFC.

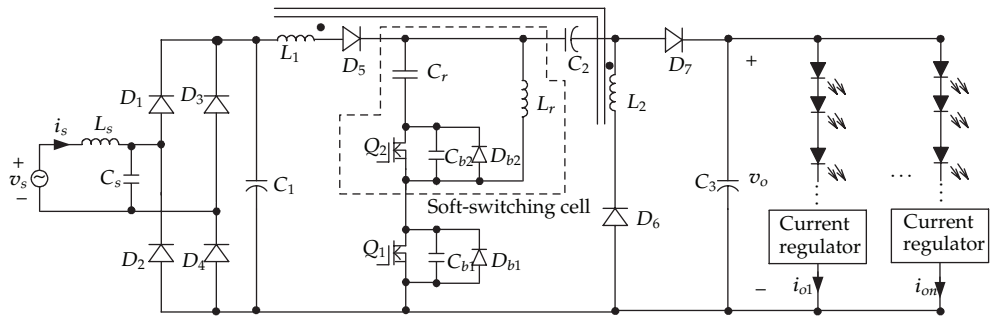

Figure 5: The proposed single-stage coupled-inductor soft-switching Sepic-type HB-LED driver.

voltage v_o can be regarded as a constant. At time $t = t_1$, this mode is ended and Q_2 is turned off. In mode 1, the voltage across the resonant inductor, v_{L_r} can be calculated by

$$v_{L_r} = \frac{(v_{C_1} - V_{D_5} - V_{DS1,\text{on}}) \cdot L_r}{L_1 + L_r}, \tag{3.1}$$

in which v_{C_1} expresses rectified half sine wave, V_{D_5} is the cut-in voltage of diode D_5, and $V_{DS1,\text{on}}$ stands for the turn-on voltage across switch Q_1. Then, inductor current i_{L_r} is determined as follows:

$$i_{L_r}(t) = i_{L_r}(0) + \int_0^t \frac{v_{C_1}(t') - V_{D_5} - V_{DS1,\text{on}}}{L_r + L_1} dt'. \tag{3.2}$$

In (3.2), the initial value of inductor current $i_{L_r}(0)$ is found by the end of mode 8.

(2) Mode 2 ($t_1 \le t < t_2$, Figure 6(b))

The switch Q_1 is turned off at t_1. The inductor L_1 discharges through the path of D_5, resonant inductor L_r, and parasitical capacitor C_{b_1}. Meanwhile, the capacitor C_2 still dumps energy to L_2, and dc load draws power from C_3. Since typical value of C_{b_1} is far smaller than the

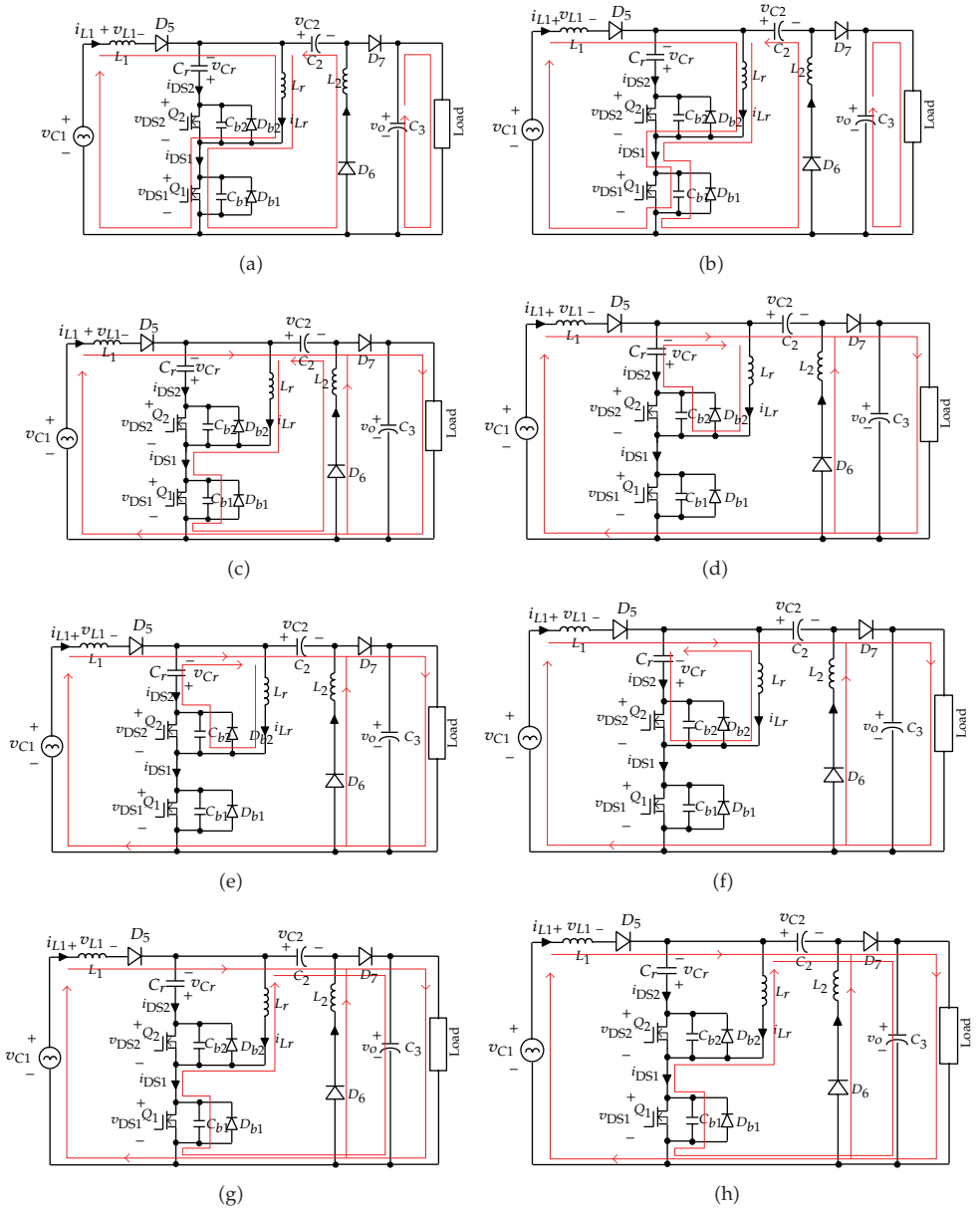

Figure 6: Equivalent circuits corresponding to the eight operation modes: (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, (f) mode 6, (g) mode 7, and (h) mode 8.

capacitance of C_2, the voltage v_{DS1} across C_{b_1} increases rapidly. Applying KVL to the loop, C_2-L_r-Q_1-D_6-L_2, one can obtain the following equivalent:

$$v_{C_2} - L_r \frac{di_{L_r}}{dt} - v_{DS1} - V_{D_6} - L_2 \frac{di_{L_r}}{dt} = 0, \tag{3.3}$$

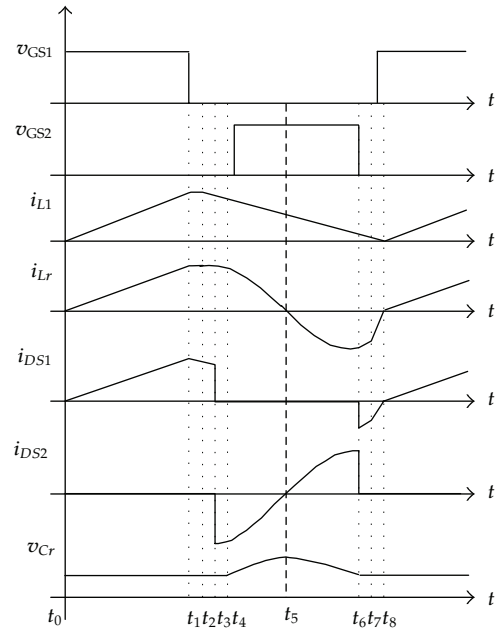

Figure 7: The related conceptual key waveforms.

in which V_{D_6} is the cut-in voltage of diode D_6. Rearranging (3.3) yields

$$i_{L_r}(t) = i_{L_r}(t_1) + \frac{1}{L_r + L_2}\int_{t_1}^{t} \left(v_{C_2}(t') - v_{DS1} - V_{D_6}\right)dt'. \tag{3.4}$$

The $i_{L_r}(t_1)$ is the initial value of i_{L_r} at mode 2, which can be found by (3.2). At $t = t_2$, the voltage v_{DS1} reaches $v_{C_2} + v_o$ and this mode is terminated.

(3) Mode 3 ($t_2 \le t < t_3$, Figure 6(c))

During this time interval, inductors L_1 and L_r still discharge energy, and voltage v_{DS1} increases. The diode D_7 starts conducting, and the voltage across L_2 is equal to output voltage v_o. Therefore, L_2 dumps energy to the output, and the inductor current i_{L_2} is expressed by

$$i_{L_2}(t) = \frac{-v_O}{L_2}(t - t_2) + i_{L_2}(t_2). \tag{3.5}$$

The capacitor C_{b_1} will be charged to $V_{\text{stress }1}$, which is also the voltage stress of Q_1. That is,

$$V_{\text{stress }1} = \left[v_{C_r} + v_{C_1} - v_{L_1}\right]_{t=t_3}. \tag{3.6}$$

(4) Mode 4 ($t_3 \le t < t_4$, Figure 6(d))

Both inductors L_1 and L_2 release energy continuously but capacitor C_2 charges. The parasitical capacitor of switch Q_2 starts dumping energy by the way of C_r and L_r until v_{DS2}

drops to zero. The resonant frequency of the loop L_r-C_{b_2}-C_r and the voltage across Q_2 can be found as follows, respectively:

$$f_{r,\text{mode }4} = \frac{1}{2\pi}\sqrt{\frac{C_{b_2}+C_r}{L_r\cdot C_{b_2}\cdot C_r}},$$

$$v_{DS2}(t) = v_{Cb_2}(t_3)\cos\left(2\pi f_{r,\text{mode }4}(t-t_3)\right) + i_{L_r}(t_3)\sqrt{\frac{L_r\cdot C_{b_2}\cdot C_r}{C_{b_2}+C_r}}\sin\left(2\pi f_{r,\text{mode }4}(t-t_3)\right). \tag{3.7}$$

(5) Mode 5 ($t_4 \le t < t_5$, Figure 6(e))

The body diode of Q_2 conducts, and inductor L_r resonates with C_r. The resonant frequency in the soft-switching cell during this mode is

$$f_{r,\text{mode }5} = \frac{1}{2\pi\sqrt{L_r\cdot C_r}}, \tag{3.8}$$

In addition, the following relationship holds:

$$L_r\frac{di_{L_r}}{dt} = -\frac{1}{C_r}\int_{t_4}^{t} i_{L_r}(t')dt' - v_{C_r}(t_4) - V_{Db_2}. \tag{3.9}$$

The V_{Db_2} is the voltage drop on the body diode D_{b_2}. According to (3.9), resonant inductor current i_{L_r} can be obtained by:

$$i_{L_r}(t) = i_{L_r}(t_5)\cos\frac{(t-t_5)}{\sqrt{L_r\cdot C_r}} - V_{C_r}(t_5)\sqrt{\frac{C_r}{L_r}}\sin\frac{(t-t_5)}{\sqrt{L_r\cdot C_r}}. \tag{3.10}$$

During this time interval, switch Q_2 is tuned on with ZVS. Operation of the driver enters into next mode as the current i_{L_r} decreases to zero.

(6) Mode 6 ($t_5 \le t < t_6$, Figure 6(f))

The energy stored in resonant capacitor C_r is dumped to L_r via Q_2. As a result, the current i_{L_r} increases negatively. In this time period, inductors L_1 and L_2 release energy but C_2 charges. At $t = t_6$, Q_2 is turned off and this mode is terminated.

(7) Mode 7 ($t_6 \le t < t_7$, Figure 6(g))

Switches Q_1 and Q_2 are off. The stored energy in the parasitical capacitor C_{b_1} is drawn by inductor L_r and v_{DS1} decreases. This mode ends when v_{DS1} drops to zero. In this mode, the inductor L_r resonates with C_{b_1} under the frequency of

$$f_{r,\text{mode }7} = \frac{1}{2\pi\sqrt{L_r\cdot C_{b_1}}}. \tag{3.11}$$

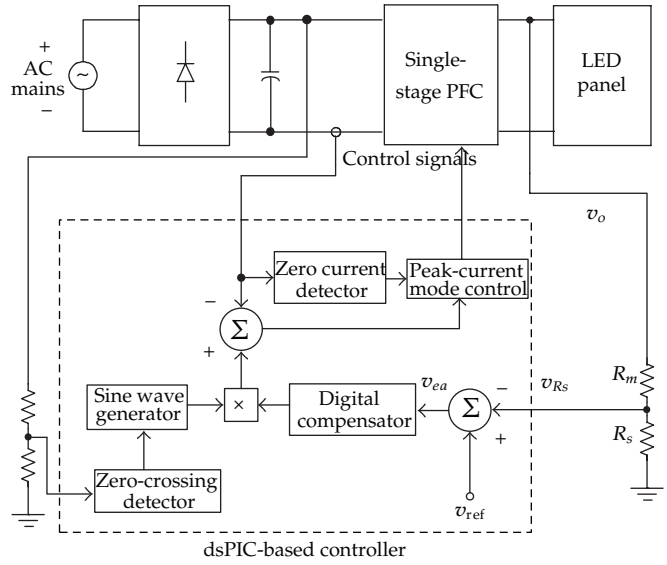

Figure 8: A block diagram to represent the control of power factor correction.

(8) Mode 8 ($t_7 \leq t < t_8$, Figure 6(h))

The energy stored in L_r is discharge by the way of C_2, D_7, C_3, and D_{b_1}. In this time interval, switch Q_1 is triggered. This mode is terminated while i_{L_1} equals zero. A complete switching cycle is ended at $t = t_8$, at which switch Q_1 has been turned on again.

4. Control of Driver

The proposed HB-LED driver not only steps down input voltage but also performs power factor correcting and functions as dimming feature. Dual-loop control and average-current control are adopted to achieve power factor correction and to regulate HB-LED current, respectively.

4.1. Control of Power Factor Correction

Figure 8 shows the block diagram of the dual-loop control. Zero-crossing point of the line voltage is detected by the zero-crossing detector, and, then, the sine-wave generator produces a unity sine wave in phase with the line voltage. In the dual-loop control, output voltage is fed back and compared with reference V_{ref} for determining the amplitude of current command. Meanwhile, input current is sensed and compared with current command for the determination of appropriate control signals driving Q_1 and Q_2. With the dual-loop control, input current shaping and output voltage regulating are readily accomplished over universal line-voltage range.

The driver operates in boundary conduction mode to perform power factor correcting. Therefore, on-time interval T_{on} of the main switch Q_1 within one switching cycle can be represented as

$$T_{\text{on}} = \frac{i_{L_1,\text{peak}}}{v_{C_1}} \cdot (L_1 + L_r). \tag{4.1}$$

The $i_{L_1,\text{peak}}$ stands for peak value of inductor current through L_1 and is obtained from

$$i_{L_1,\text{peak}} = 2I_{\text{PK}}\left|\sin(2\pi f_L t)\right|. \tag{4.2}$$

In (4.2), f_L is the line frequency and I_{PK} expresses the amplitude of line current. In addition, off-time interval T_{off} of the main switch Q_1 within one switching cycle is found by

$$T_{\text{off}} = \frac{i_{L_1,\text{peak}}}{v_{C_2} + v_o - v_{C_1}} \cdot L_1. \tag{4.3}$$

Suppose that voltage drop on the input diodes can be neglected. Thus, v_{C_1} can be expressed as

$$v_{C_1} = V_P\left|\sin(2\pi f_s t)\right|, \tag{4.4}$$

where V_P is the amplitude of line voltage. From (4.1)–(4.4), determination for T_{on} and T_{off} of a control signal can be further derived and becomes

$$\begin{aligned} T_{\text{on}} &= \frac{2I_{\text{PK}}}{V_P} \cdot (L_1 + L_r), \\ T_{\text{off}} &= \frac{2I_{\text{PK}}\left|\sin(2\pi f_L t)\right|}{v_{C_2} + v_o - V_P\left|\sin(2\pi f_L t)\right|} \cdot L_1. \end{aligned} \tag{4.5}$$

Since the switching frequency of the driver, f_{sw} , is

$$f_{\text{sw}} = \frac{1}{T_{\text{on}} + T_{\text{off}}}, \tag{4.6}$$

with the relationships of (4.5), expression for f_{sw} is rewritten as

$$f_{\text{sw}} = \frac{V_P\left(v_{C_2} + v_o - V_P\left|\sin(2\pi f_L t)\right|\right)}{2I_{\text{PK}}\left((v_{C_2} + v_o)(L_1 + L_r) - (L_1 + L_r - 1)\left(V_P\left|\sin(2\pi f_L t)\right|\right)\right)}. \tag{4.7}$$

4.2. Dimming Control of HB-LED Panel

Each string current of HB-LED panel is controlled by current regulator to achieve current sharing and dimming feature. The current regulator mainly includes an active switch and

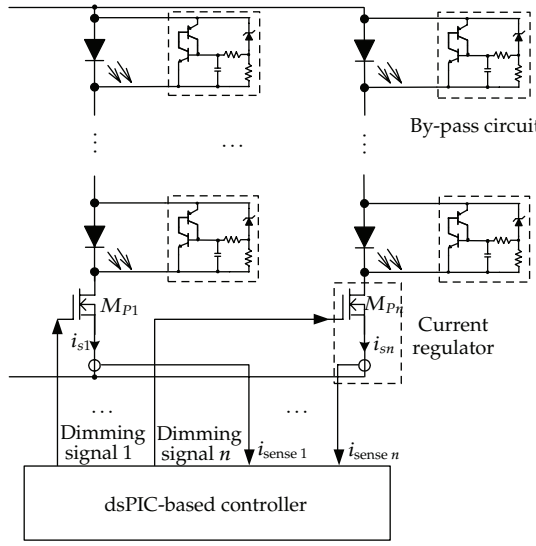

Figure 9: The HB-LED panel with current regulators and by-pass circuits.

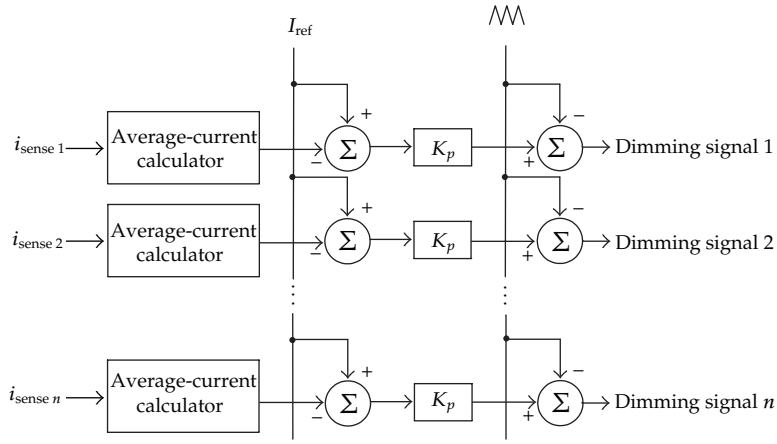

Figure 10: A block diagram to represent the control for LED panel.

a current sensor, as shown in Figure 9. String current is sensed, and, then, according to its average value the duty ratio of the active switch is determined so as to accomplish 400 Hz burst-mode current control. Consequently, string current can be controlled to achieve luminance balance and dimming feature. The associated average-current calculation and dimming signal determination are all-digital implementation, of which control block diagram is illustrated in Figure 10.

In Figure 9, duty ratio of the active switch in the jth LED string, $D_{\text{dim},j}$, can be expressed as

$$D_{\text{dim},j} = \frac{T_{\text{dim,on},j}}{T_{\text{dim}}}, \tag{4.8}$$

where T_{dim} denotes the period of dimming signal and $T_{\text{dim,on},j}$ is the on-state time interval of the active switch in the jth LED string. In Figure 10, average value of the jth-string sensed current is calculated by

$$I_{s,j} = \frac{1}{T_{\text{dim}}} \int_0^{T_{\text{dim,on},j}} i_{s,j}(t)dt. \tag{4.9}$$

Additionally, while the jth active switch is closed, a corresponding current through the jth LED string has to be

$$I_{\text{LED,on},j} = \frac{v_O - N_j \cdot V_{f,\text{LED}}}{N_j \cdot R_d}. \tag{4.10}$$

In (4.10), N_j is the total number of LEDs in the jth string; $V_{f,\text{LED}}$ and R_d are the forward voltage and equivalent series resistance of LED, respectively. Since $I_{s,j}$ can be also evaluated by

$$I_{s,j} = D_{\text{dim},j} \cdot I_{\text{LED,on},j}, \tag{4.11}$$

then, from (4.9)-(4.11) the following equivalent holds:

$$D_{\text{dim},j} = \frac{N_j \cdot R_d}{T_{\text{dim}}\left(v_o - N_j \cdot V_{f,\text{LED}}\right)} \int_0^{T_{\text{dim,on},j}} i_{s,j}(t)dt. \tag{4.12}$$

Based on (4.12), to determine $D_{\text{dim},j}$, the values of R_f and $V_{f,\text{LED}}$ should be given in advance, which leads to the determination error caused from the aging effect of LED. To avoid the drawback, the difference between the average sensed current $I_{s,j}$ and a reference current I_{ref} is amplified and then compared with a triangular waveform so as to fulfill pulse-width-modulation (PWM) current control, as shown in Figure 10. The corresponding control law can be expressed as follows:

$$D_{\text{dim},j} = \frac{V_{\text{tri,peak}}/2 + K_p\left(I_{\text{ref}} - I_{s,j}\right)}{V_{\text{tri,peak}}}, \tag{4.13}$$

where $V_{\text{tri,peak}}$ is the peak value of the triangular waveform and K_p stands for a constant. The $D_{\text{dim},j}$ is in the range of 0-1.

In this paper, a by-pass circuit is also presented, which is in parallel with LED, as shown in Figure 9. While LED being out of order, it is triggered and provides an alternative path to continue string current. As the presented by-pass circuit conducts, voltage drop across its terminals is about 1 V. Compared with conventional single-zener-diode by-pass circuit, of which conduction voltage drop is larger than 3.3 V, the power dissipation of the presented by-pass circuit is much smaller than that of the conventional one.

5. Design Considerations

The inductances and capacitances, L_1, L_2, C_2, and C_3, influence the performances of the single-stage driver significantly. Determinations for L_1 and L_2 are presented as follows:

$$L_1 = \frac{L_{l_1}L_{l_2} + L_mL_{l_1} + n^2L_mL_{l_2}}{L_{l_2} - (n-1)L_m},$$
$$L_2 = \frac{L_{l_1}L_{l_2} + L_mL_{l_1} + n^2L_mL_{l_2}}{L_{l_1} + n(n-1)L_m}, \tag{5.1}$$

in which n is the turns ratio of the coupled inductors, L_m denotes the magnetizing inductance, and L_{l_1} and L_{l_2} stand for leakage inductances of winding 1 and winding 2, respectively. In addition, the capacitances C_2 and C_3 are obtained by

$$C_2 = \frac{L_e}{\Delta V_{C_1(\max)}} \cdot \frac{I_{\mathrm{PK}}^2}{2} \cdot \frac{1}{\left(V_o + \sqrt{2}V_{\mathrm{AC(min)}}\right)},$$
$$C_3 = \frac{I_o}{2 \cdot \pi \cdot f_L \cdot \Delta V_o}, \tag{5.2}$$

where L_e equals $L_{l_1} // L_{l_2}$, V_o and ΔV_o represent dc-bus voltage and its ripple component, in turn, and $V_{\mathrm{AC(min)}}$ expresses the rms value of the minimum line voltage. The peak value of the inductor current i_{L_1} can also be expressed as follows:

$$i_{L_1,\mathrm{peak}}(t) = \frac{V_P T_{\mathrm{on}} \left|\sin(2f_L\pi t)\right|}{L_1}. \tag{5.3}$$

Then, the filtered input current is determined by

$$\begin{aligned} \left|i_{s,\mathrm{filtered}}(t)\right| &= \frac{2}{T_s}\int_0^{T_s/2} i_{L_1}(t)dt \\ &= \frac{2V_pT_{\mathrm{on}}}{T_s \cdot (L_1 + L_r)\left(f_L \cdot \pi\right)}. \end{aligned} \tag{5.4}$$

In addition, the power drawn from line voltage can be computed in the following:

$$\begin{aligned} P_{\mathrm{in}} &= \frac{2}{T_s}\int_0^{T_s/2} v_s(t) \cdot i_{s,\mathrm{filtered}}(t)dt \\ &= \frac{2V_p^2T_{\mathrm{on}} + T_s(L_1 + L_r)}{T_s \cdot (L_1 + L_r)\left(f_L \cdot \pi\right)}. \end{aligned} \tag{5.5}$$

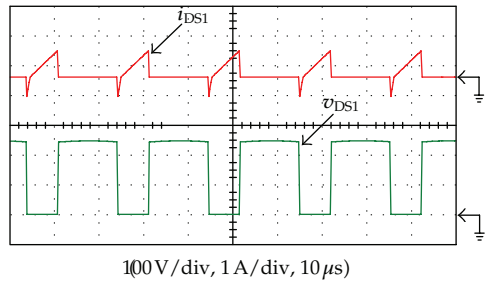

Figure 11: Voltage and current waveforms of switch Q_1.

In Figure 8, the output voltage v_o is divided by the two resistors, R_m and R_s, with 1% accuracy such that the voltage v_{R_s} can be described as

$$v_{R_s} = v_o \frac{R_s(1 \pm 1\%)}{R_s(1 \pm 1\%) + R_m(1 \pm 1\%)}. \tag{5.6}$$

Suppose that a 10-bit analog-to-digital converter (ADC) is used. Therefore, the ADC resolution is calculated as

$$\text{Resolution} = \frac{\text{Supply Voltage}}{\text{10-bit ADC}} = \frac{5}{2^{10}} \cong 0.00488\,(\text{V}). \tag{5.7}$$

Thus, the maximum deviation of v_{R_s} after analog-to-digital conversion is

$$v_{R_s,\text{con}}|_{\max} = v_{R_s} \pm 0.0048. \tag{5.8}$$

Accordingly, the deviation on the output voltage, Δv_o, can be found by

$$\Delta v_o = \pm 0.0048 \frac{R_s(1 \pm 1\%) + R_m(1 \pm 1\%)}{R_s(1 \pm 1\%)}. \tag{5.9}$$

6. Simulations and Hardware Measurements

A prototype of the proposed HB-LED driver is built to demonstrate the theoretical analysis and to verify the feasibility, of which controller is implemented on a 16-bit disPIC-30F4011 chip. The adopted microcontroller comprises a 10-bit ADC with conversion rate up to 500 Ksps, 9 input channels, 6 PWM outputs, and 5 16-bit timers. It fulfills the controlling of power factor correction, current sharing, and dimming. The driver has been designed according to the following specifications:

input voltage: 85 ~ 265 V,

output power: 100 W,

output current: 1.75 A,

output voltage: 58 V,

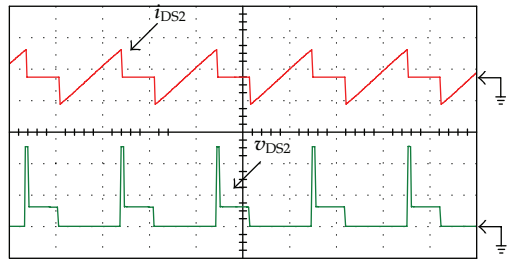

Figure 12: Voltage and current waveforms of switch Q_2.

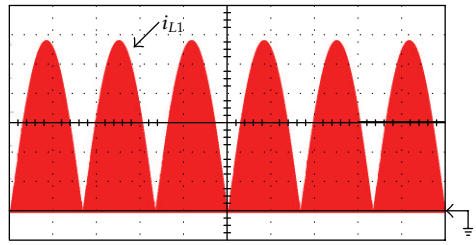

Figure 13: The current waveform of the inductor L_1.

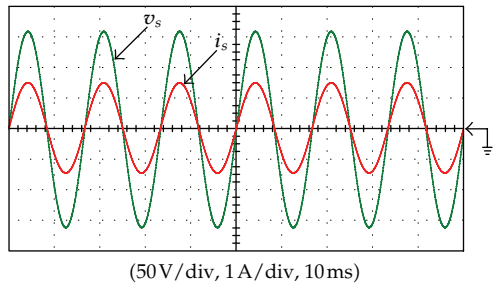

Figure 14: Line voltage and input current when mains voltage is 110 V.

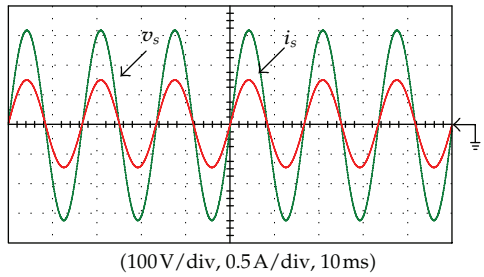

Figure 15: Line voltage and input current when mains voltage is 220 V.

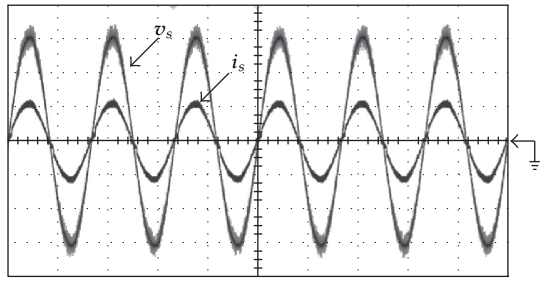

Figure 16: Practical results of line voltage and input current.

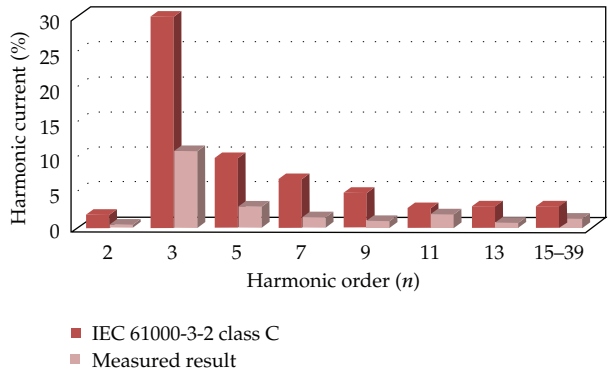

Figure 17: Measured input current harmonics.

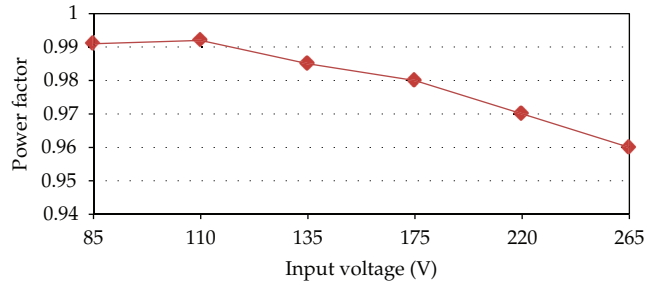

Figure 18: Power factor measurement over universal-line input range.

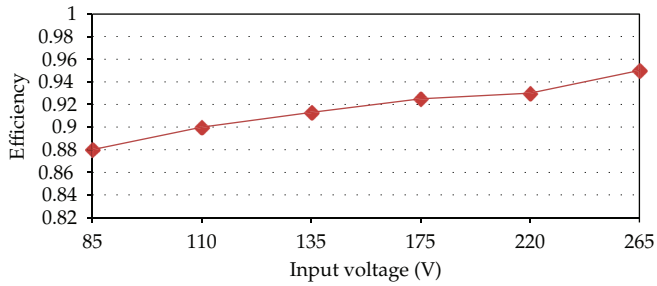

Figure 19: Measured efficiency over universal-line input range.

LED: LUMILEDS 1.2 W/3.42 V/0.35 A,

LED panel: 5 strings, 17 pieces in series for each string.

Component values and important parameters are determined as:

Q_2: IRF730 (400 V/5.5 A),

Q_1: 17N80C3 (800 V/17 A),

$L_1 = 1.2$ mH, $L_2 = 0.77$ mH, $L_r = 0.1$ mH,

$C_1 = 0.1\,\mu$F, $C_2 = 0.25\,\mu$F, $C_3 = 100\,\mu$F, and $C_r = 0.05\,\mu$F.

Figure 11 is the waveforms of voltage and current of the main switch Q_1, while Figure 12 shows the waveforms of Q_2 in the soft-switching cell. From Figures 11 and 12, it can be observed that zero-voltage switching (ZVS) feature is achieved by the both switches Q_1 and Q_2. Figure 13 is the simulated waveform of the current i_{L_1}. Figure 14 shows the simulated line voltage and input current when mains voltage is 110 V. For 220 V mains input, the simulated line voltage and input current are shown in Figure 15. Figure 16 shows the hardware measurement of line voltage and input current while mains voltage is 110 V. From Figures 13–16, it can be found that a unity power factor is achieved by the single-stage HB-LED driver. Figure 17 shows the harmonics of the input current measured by PM3000 and then compared with IEC6100-3-2 class C. From Figure 17, it can be observed that the line current harmonics are much less than the requirements of the standard. Power factor and efficiency measurements are shown in Figures 18 and 19, in turn, illustrating that high power factor and efficiency can be achieved by the single-stage HB-LED driver.

7. Conclusion

This paper has proposed a single-stage Sepic-type soft-switching HB-LED driver with coupled inductor for universal line input. The proposed driver not only can perform power factor correcting but also achieve zero-voltage switching feature and step down input voltage directly. Consequently, a unity power factor is obtained and efficiency is improved. In the driver, its output voltage can be much smaller than the ac-side voltage, reducing component stresses significantly. Therefore, the driver is suitable for the applications of high-line voltage and/or low output voltage. To drive LED panel, an all-digital controller is also presented for power factor correcting, dc-bus voltage regulating, current sharing, and LED dimming, which is implemented on a 16-bit disPIC chip. A prototype of the designed single-stage driver to ballast 100 W 58 V HB-LED panel has been built. The simulations and practical measurements have verified the feasibility and features of the single-stage HB-LED driver.

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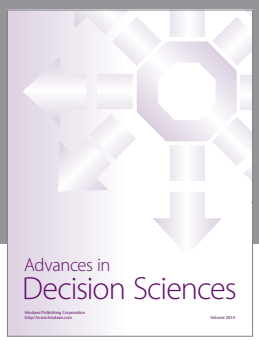

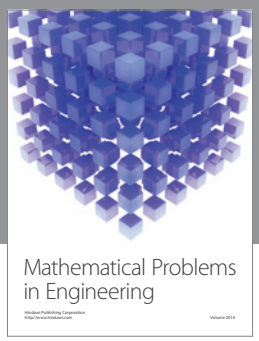

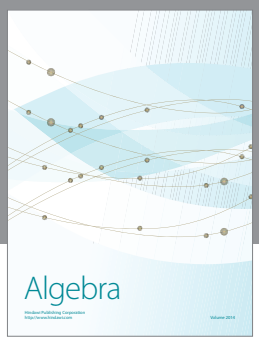

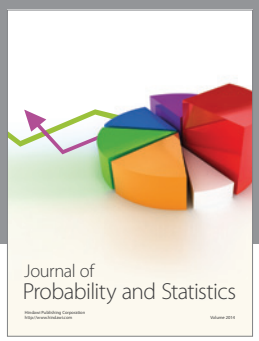

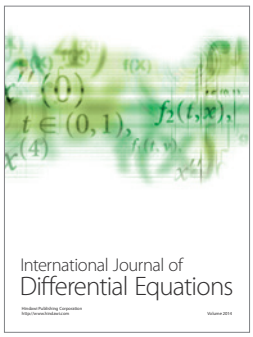

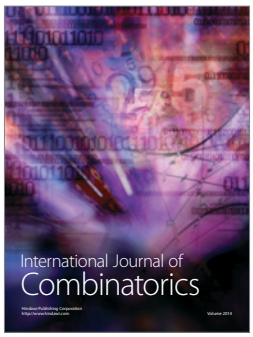

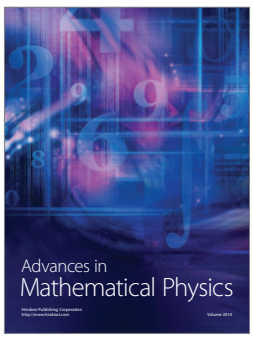

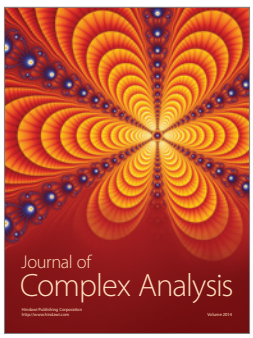

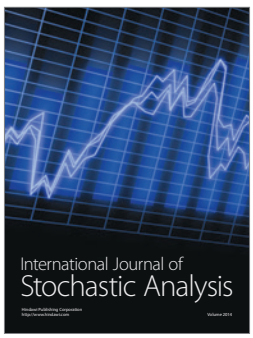

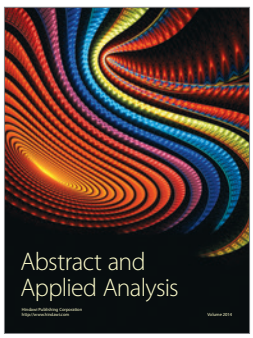

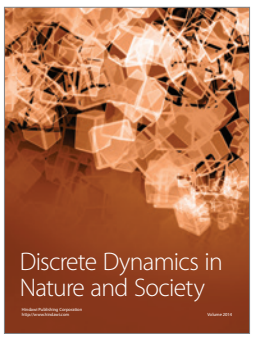

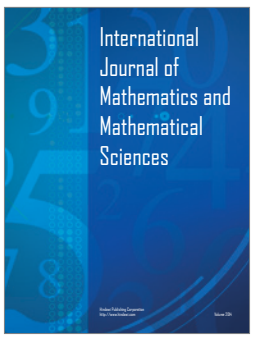

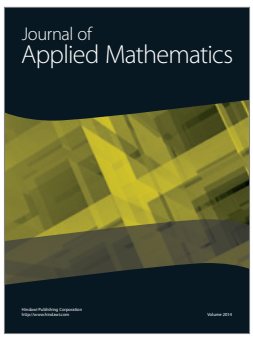

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